



CONTROL OF HEAT AND CHARGE TRANSPORT IN NANOSTRUCTURED HYBRID MATERIALS

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Final Report

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Control of Heat and Charge Transport in Nanostructured Hybrid Materials

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Abstract

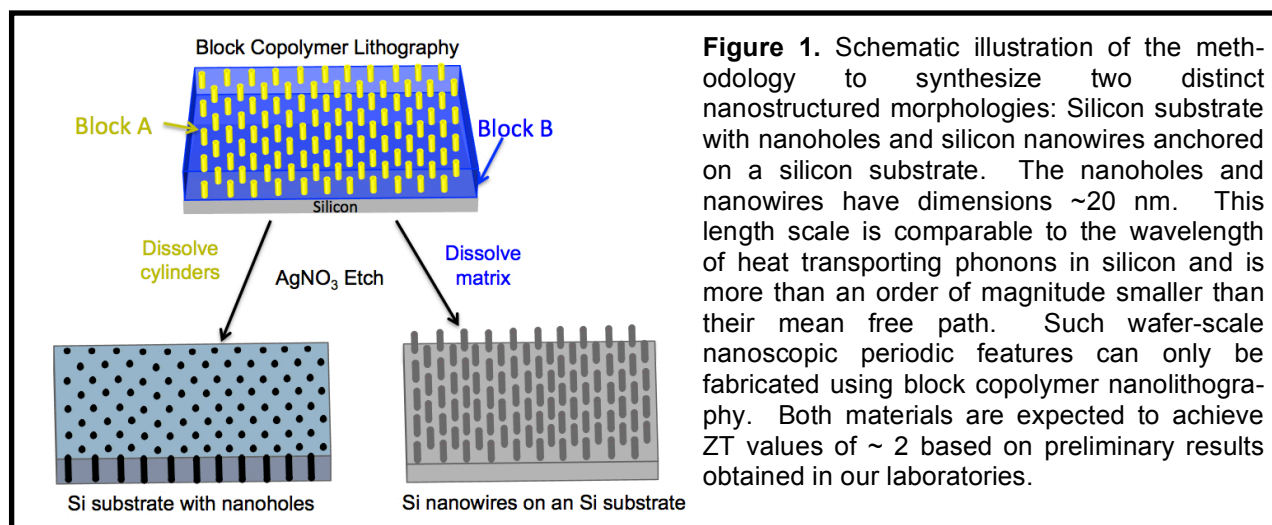
The proposed research efforts focused on the wafer-scale manufacture of silicon based thermoelectric modules with $ZT > 2$. Recent measurements in our groups have yielded device ZT values of 0.4 on thermoelectric modules consisting of vertically oriented silicon nanowires. This is the highest reported ZT for a silicon based thermoelectric module. Based on this work, here, we aimed to develop nanostructured thermoelectric modules utilizing two different silicon morphologies: 1. Deep nanoholes in bulk silicon with aspect ratio's exceeding 10,000 and 2. Extremely long silicon nanowires with aspect ratio's exceeding 10,000. Temperature differences as high as 800 °C are achievable for both types. The bulk nanostructured silicon modules were produced using block copolymer nanolithography, which is a polymer-based nanotemplating technique. This technique is amenable to roll-to-roll processing making wafer-scale manufacturing of bulk nanostructured silicon thermoelectrics practical. In fact, the cost of block copolymer is comparable to the cost of standard photoresists. Our current ability to reach ZT values ~ 0.4 is a direct consequence of the dramatically low thermal conductivity of the silicon nanostructures. Specifically, experiments on an array of 20 nm diameter vertically oriented silicon nanowires have demonstrated thermal conductivities $k \sim 0.4$ W/m-K, which is below the amorphous limit. The major challenge that is limiting ZT values to ~ 0.4 is the elimination of electrical contact resistance.

Introduction

Thermoelectric materials have the potential to recycle waste heat, wherever it is found, directly into useful electric power. However, most thermoelectric materials in current use suffer from low efficiency and high cost. The figure of merit, ZT , for bulk thermoelectric materials has values near 1, which corresponds to an overall efficiency of $\eta \sim 6 - 8\%$ at nominal operating temperatures.

Nanostructured silicon, the material of choice in this work, is uniquely suited for use as a bulk thermoelectric material for waste heat recovery as: **a.** Previous experiments from our group have shown that nanostructured silicon's thermal conductivity is two orders of magnitude smaller than bulk silicon.¹ **b.** All practical thermoelectric devices must use p- and n-type materials.² The p- and n-type materials are connected electrically in series and connected thermally in parallel.³ Silicon, is easily doped with both p- and n-type carriers. **c.** Unlike other thermoelectric materials, silicon has the advantage of being an earth abundant material. **d.** Thermoelectrics based on silicon can easily leverage existing semiconductor manufacturing and processing facilities. Consider that the worldwide silicon production exceeded 6 million metric tons in 2008; and **e.** Silicon can easily withstand temperatures exceeding 1000°C.

This work focused on the development of commercially viable silicon based thermoelectric modules. The techniques developed in our groups allow for wafer-scale manufacture of silicon nanostructures (nanoholes and nanowires) for high efficiency thermoelectric modules, with efficiencies $> 15\%$. Experiments in our groups have shown that a wafer-scale array of vertically oriented 20 nm diameter silicon nanowires (Fig. 2C) have extremely low thermal conductivities ~ 0.4 W/m-K, yielding ZT values ~ 0.4 . Note that this is the highest ZT value ever reported for a bulk silicon-based thermoelectric module. In comparison the ZT value for bulk silicon is ~ 0.01 . Currently, the predominant factor limiting ZT in our thermoelectric modules is the parasitic electrical contact resistance. By significantly reducing this contact resistance, we believe that thermoelectric module ZT values greater than 2 are achievable through the techniques discussed below.

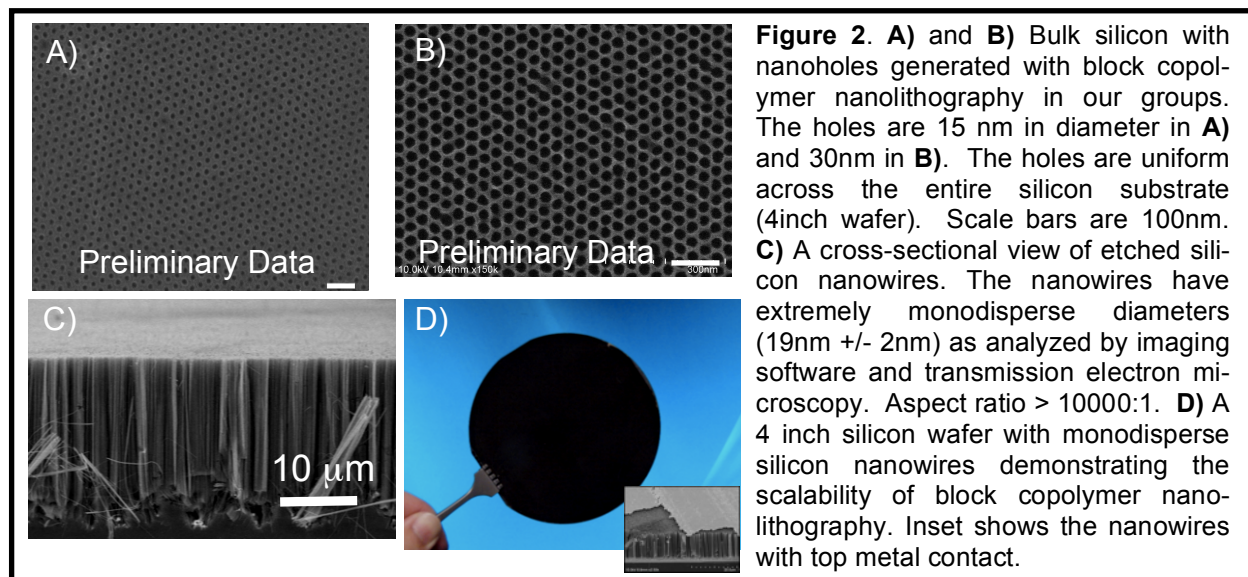


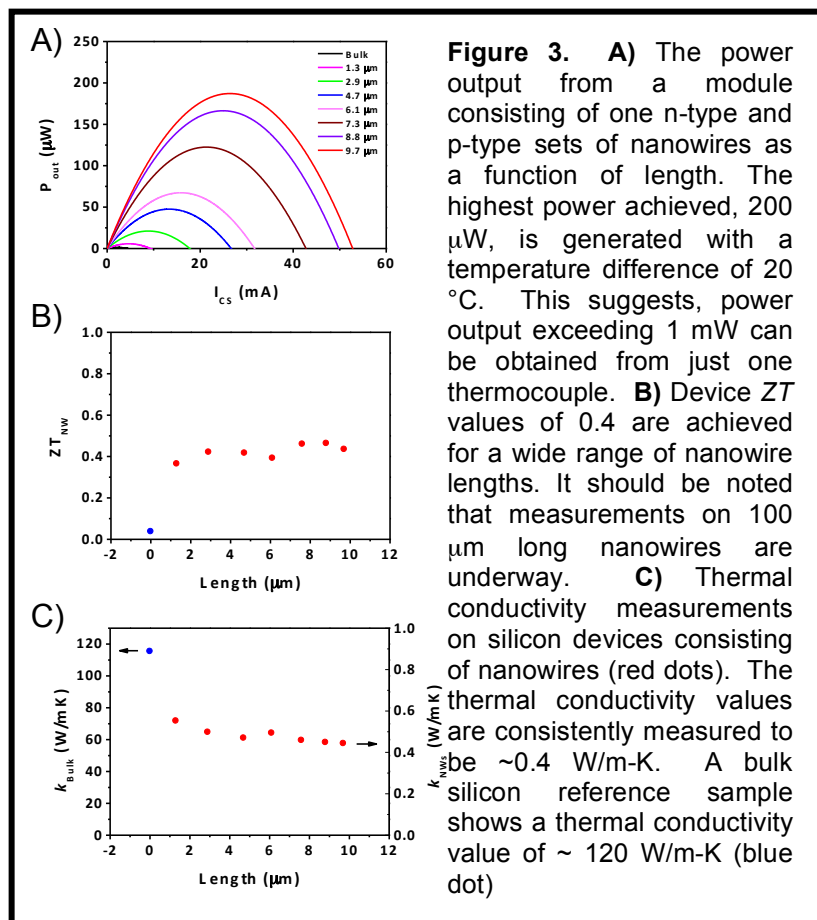
Overall, the major tasks developed included 1. Fabrication of bulk silicon nanostructures with different morphologies (nanoholes or nanowires) using block copolymer nanolithography and a deep electroless etch (Figure 1). 2. Measurement and optimization of ZT for both p-type and n-type silicon nanostructures. 3. Development of thermoelectric modules consisting of p-type and n-type silicon nanostructures connected electrically in series and thermally in parallel. 4. Optimization of the electrical contact resistance and power factor to allow $ZT > 2$.

Technical Approach and Results

The majority of heat transporting phonons in inorganic materials such as silicon have wavelengths or mean free paths at the nanoscale ($\lambda \sim 1 - 500$ nm).⁴ Therefore, the development of a nanostructured material with periodically arranged nanoscale features with dimensions $\sim 1 - 50$ nm should dramatically scatter phonons. Commonly available fabrication techniques do not allow for the nanoscale resolution required. For example, the inherent limitation of light due to the diffraction limit precludes the use of common photolithographic techniques.⁵ These limitations can be overcome through the use of electron-beam lithographic (EBL) processes. However, EBL is an expensive and serial process that limits the size of the lithographically defined region. In addition, EBL suffers from “exposure bleed”, which limits the pitch between any nanoscale features to ~ 50 nm.⁶

In comparison, block copolymer lithography, the approach utilized in this work, is a scalable technique that is amenable to roll-to-roll processing. It utilizes molecular self-assembly, in combination with standard photolithographic processes, to generate monodisperse, nanoscopic inclusions, $\sim 5 - 50$ nm in scale.⁷⁻¹⁹ The inclusion pitch for the nanoholes and nanowires in this work ranged from $10 - 15$ nm (see Fig. 2A and 2B), resulting in materials with thermal conductivities at or below the amorphous limit.²⁰





To generate bulk nanostructured materials, we developed an electroless electrochemical etch was utilized to etch deep (hundreds of microns) holes into a silicon wafer using the block copolymer as a mask.²¹ This electrochemical etch is highly anisotropic, resulting in nearly vertically etched nanoholes or nanowires with aspect ratios in excess of 10,000:1 (see Fig. 2C). This allows for the development of 3D bulk nanostructured silicon substrates.

Measurements on p- and n-type bulk silicon nanowire devices were performed in our laboratory (Figure 3). These measurements have yielded device ZT values of 0.4, which is the highest value measured in a bulk silicon device. The ZT

is expected to increase above 2 when parasitic contact resistances are eliminated, as discussed below.

Using 4-point probes and various contact materials, we identified best approaches for making ohmic and low thermally resistive contacts to silicon thin films, and then translate those results to nanohole and nanowire structures. One strategy was to use shadow masks over the block copolymer template to pattern highly doped, non-nanopatterned regions for monolithic contacts, thus ensuring a smooth translation of the thin film findings to the nanohole materials, since both will have the same contacts

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